ABSTRACT OF THE DISCLOSURE

A clock-generating circuit for forming internal clock signals by comparing a signal obtained by delaying, through a variable delay circuit, an input clock signal input through an external terminal with the input clock signal through a phase comparator circuit, and so controlling the delay time of the variable delay circuit that they are brought into agreement with each other, wherein the clock-generating circuit and an internal circuit to be operated by the clock signals formed thereby are formed on a common semiconductor substrate, and an element-forming region in which the clock-generating circuit is formed is electrically isolated from an element-forming region in which the digital circuit is constituted on the semiconductor substrate relying upon the element-isolation technology. The power-source passages, too, are formed independently of other digital circuits.